

Surface Mount Clock Oscillator

- High frequency range
- Tight stability available

Part Numbering Example: **WU33AQ - XX.XXXX M**

W		U	33	A	Q		XX.XXXXM
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	SYMMETRY	OPERATING TEMP.	STABILITY	FREQUENCY
W	Blank=Cmos T = TTL	O = Full Size OH = Half Size U = 5X7 S = 3.2X5	18= 1.8V 25= 2.5V 33= 3.3V 50= 5.0V	Blank=40/60% A=45/55%	N= -55 °C +105°C Q= -55 °C +125°C (MIL-STD-883B) M= -55 °C +125°C (MIL-PRF-55310D)	Blank = ±50ppm 2 = ±25ppm 3 = ±20ppm	0.50 ~200.000 MHz

Specifications:

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Description	Min	Typ	Max	Unit
Frequency Range: Programmable to Any Discrete Frequency	0.5		133.000	MHz
Available Stability Options:	-50 -25 -20		50 25 20	ppm ppm ppm
Programmable Supply Voltage: (1–133 MHz)	4.5	5.0	5.5	V
(1–100 MHz)	3.0	3.3	3.6	V
Operating Temperature Range Options:	-40 -55 -55		+85 +105 +125	°C
Storage Temperature:	-55			
Aging (PPM/Year) Ta=25C, Vdd=5/3.3V			±3	ppm
Programmable Output Level:	TTL/Cmos			

Operating Conditions:

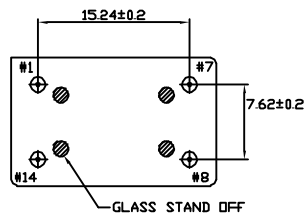
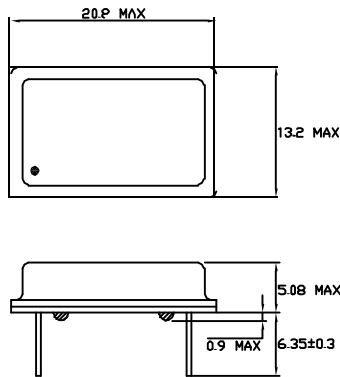
Description	Unit
Vdd Supply Voltage	3.0 5.5 V
C _{TTL} Max Capacitive Load on outputs for TTL levels	
4.5V–5.5V Vdd ≤ 40 MHz	50 pF
4.5V–5.5V Vdd > 40–133 MHz	25 pF
C _{CMOS} Max Capacitive Load on outputs for CMOS levels	
4.5V–5.5V Vdd, ≤ 66 MHz	50 pF
4.5V–5.5V Vdd, >66–200MHz	25 pF
2.25V–3.6V Vdd, ≤ 40 MHz	30 pF
2.25V–3.6V Vdd, >40–200MHz	15 pF
1.62V–1.89V Vdd, ≤ 40 MHz	25 pF
1.62V–1.98V Vdd, >40–200MHz	15 pF

Environmental And Mechanical	
Mechanical Shock	Per MIL-STD-883 ,Method 2002 ,Cond.B
Thermal Shock	Per MIL-STD-883 ,Method 1011 ,Cond.A
Vibration	Per MIL-STD-883 ,Method 2007 ,Cond.A
Seal	Per MIL-STD-883, Method 1014, Condition B & C
Solderability	Per MIL-STD-883 ,Method 2003 ,Cond.A

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Style O Full Size 14 Pin Dip

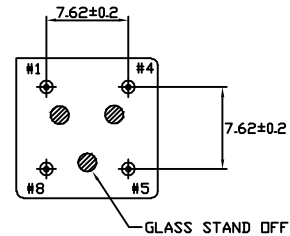
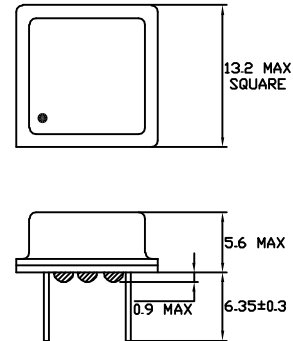
STYLE 1 FULL SIZE 14 PIN DIP



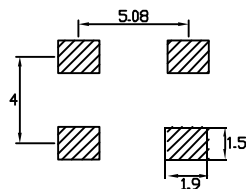
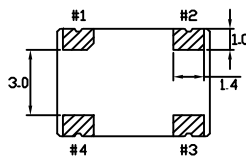
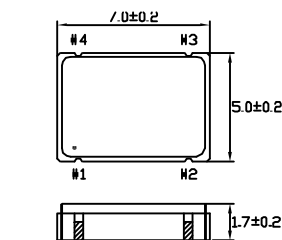
PIN FUNCTION
 1 CONTROL
 7 GND
 8 OUTPUT
 14 Vdd

Style OH Half Size 8 Pin Dip

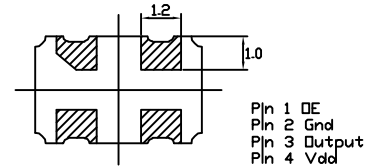
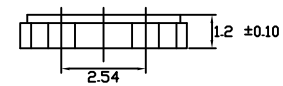
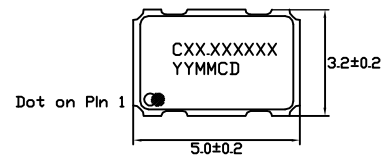
STYLE 4 HALFSIZE 8 PIN DIP



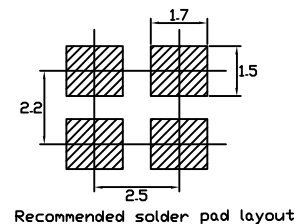
PIN FUNCTION
 1 CONTROL
 4 GND
 5 OUTPUT
 8 Vdd

Style U 5x7 Ceramic SMD

PIN FUNCTION
 1 CONTROL
 2 GND
 3 OUTPUT
 4 Vdd

Style G 3.2x5 Ceramic SMD

Pin 1 OE
 Pin 2 Gnd
 Pin 3 Output
 Pin 4 Vdd



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Electrical Characteristics

Description	TEST CONDITIONS	Min	Typ	Max	Unit
Input Characteristics (Pin 1):					
V _{IL} , Low-Level Input Voltage	4.5–5.5V V _{DD}			0.8	V
TO DISABLE OUTPUT	1.62–3.6V V _{DD}			0.2V _{DD}	V
V _{IH} , High-Level Input Voltage	4.5–5.5V V _{DD}	2.0			V
TO ENABLE OUTPUT OPEN	1.62–3.6V V _{DD}	0.7V _{DD}			
I _{IL} , Input Low Current	V _{IN} = 0V			10	μA
I _{IH} , Input High Current	V _{IN} = V _{DD}			5	μA
Output Characteristics:					
V _{OL} , Low-Level Output Voltage	4.5V–5.5V V _{DD} , 16 mA I _{OL}			0.4	V
	1.62V–3.6V V _{DD} , 8 mA b _L			0.4	V
V _{OHTTL} , High-level Output Voltage TTL	4.5V–5.5V V _{DD} , -16 mA I _{OL}	2.4			V
V _{OHCMS} , High-level CMOS Voltage	4.5V–5.5V V _{DD} , -16 mA I _{OL}	V _{DD} -0.4			V
	1.62V–3.6V V _{DD} , -8 mA b _L	V _{DD} -0.4			V
Power Supply Current:				45	mA
(unloaded)				25	mA
4.5–5.5 V _{DD} , OUTPUT FREQ ≤ 133 MHz					
1.62–3.6 V _{DD} , OUTPUT FREQ ≤ 200 MHz					
Standby Current:			10	50	μA
Pull-Up (Pin 1)					
4.5–5.5 V _{DD} , V _{IN} = 0V		1.1	3.0	8.0	MΩ
4.5–5.5 V _{DD} , V _{IN} = 0.7V		50	100	200	KΩ
Tri-State Leakage Current			20		μA
Output Enable Mode:		Output is Tri-States			

Output Clock Switching Characteristics

Description	TEST CONDITIONS	Min	Typ	Max	Unit
Duty Cycle:					
TTL @ 1.4 V	≤ 50 MHz, C _L = 50 pF	45		55	%
4.5-5.5 Vdd	50–66 MHz, C _L = 15 pF	45		55	%
	66–125 MHz, C _L = 25 pF	45		55	%
	125–200 MHz, C _L = 15 pF	45		55	%
Duty Cycle:					
CMOS @ Vdd/2	≤ 66 MHz, C _L ≤ 25 pF	45		55	%
4.5-5.5 Vdd	66–125 MHz, C _L ≤ 25 pF	45		55	%
1.62–3.6 Vdd	125–200 MHz, C _L ≤ 15 pF	45		55	%
	≤ 40 MHz, C _L ≤ 30 pF	45		55	%
	40-200 MHz, C _L ≤ 15 pF	45		55	%
Output Clock Rise/Fall	0.8V–2.0V, 4.5-5.5 Vdd, C _L = 50			1.8	ns
	0.8V–2.0V, 4.5-5.5 Vdd, C _L = 25			1.2	ns
	0.8V–2.0V, 4.5-5.5 Vdd, C _L = 15			1.3	ns
	0.2–0.8Vdd, 4.5-5.5 Vdd, C _L = 50			3.4	ns
	0.2–0.8Vdd, 1.62–3.6 Vdd, C _L = 30			4.0	ns
	0.2–0.8Vdd, 1.62–3.6 Vdd, C _L = 15			2.4	ns
Start Up Time	From power on			2	ms
Output Disable Time					
Synchronous	OE pin LOW to output Hi-Z		T/2	T+10	ns
Asynchronous	T = Frequency oscillator period		10	15	ns
Output Enable Time				50	ns
RMS Period Jitter:			5	10	ps

* Jitter tested at > 1,000,000 samples, exceeding JEDEC std JESD65.